

**METHOD FOR USING A HARD MASK  
FOR CRITICAL DIMENSION GROWTH CONTAINMENT**

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**Field of the Invention:**

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The present invention is directed to a method for minimizing and containing the critical dimension growth of a feature on a semiconductor wafer and any other product, such as for example, the magnetic head for a disk drive and a flat panel display, which could be constructed using semiconductor processing techniques.

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**Background of the Invention:**

The critical dimension (CD) of a feature on a semiconductor wafer, or any product fabricated using semiconductor processing techniques, is a width of that feature. The pitch is generally defined as a critical dimension plus the distance to the next feature.

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For semiconductor process methods using etch techniques, lithographic masking layers, such as for example photoresist layers, can be formed on top of the material to be etched. Photoresist layers define the desired features, masking the portion of underlying layer which is not to be etched, and leaving exposed the portion to be etched. During the etching process, materials from a portion of the layer which is etched, as well as compounds formed by various combinations of the etchant gases, the lithographic mask, and the materials of the layer to be etched, can tend to coat the sides of the desired feature, and the lithographic mask, and thereby increase the critical dimension of the feature beyond that defined immediately under the lithographic mask.

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Such growth of the critical dimension can disadvantageously diminish

the space between the features and thereby adversely affect the functionality of the features.

As is known in the art, lithographic masks can include by way of example only, (i) soft masks such as photoresist masks, e-beam resist masks, x-ray resist masks, and syncotron particle acceleration resist masks, and (ii) hard masks, such as metals and oxides of metals such as silicon dioxide ( $\text{SiO}_2$ ). However, such soft and hard masks have not been found to be particularly useful in controlling the critical dimension growth.

Accordingly, there is a need to provide a semiconductor processing methodology which allows for the desired features to be appropriately etched without causing a growth of the critical dimension of the feature during the etching process.

#### Summary of the Invention:

The present invention provides for a methodology which allows for etching the features while controlling or minimizing the growth of the critical dimension of the feature during the etching process. The method is useful for fabricating semiconductor wafers in order to produce chip products, magnetic heads for disk drives, and flat panel displays, by way of example only.

The method for critical dimension growth containment includes placing a wafer with a hard mask comprised of a reactive metal, deposited over a layer to be etched in a reactor and etching the wafer in the reactor. The placing step further includes placing a hard mask which is comprised of a reactive metal <sup>or</sup> an oxide, nitride, fluoride, carbide, boride, or some combination of an oxide, nitride, fluoride, carbide, and/or boride of a reactive metal. Such combination could include, by way of example only, an oxinitride, oxiboride, oxifluoride or

oxycarbide, of a reactive metal or any other combination or compound formed by exposing a reactive metal to ions or radicals of any combinations of oxygen, nitrogen, fluorine, boride, and/or carbon.

5 The placing step further includes placing a wafer having a hard mask which is comprised of one of titanium, aluminum, tantalum, tungsten, cobalt, or molybdenum, or an oxide, nitride fluoride carbide or boride of said reactive metals.

The hard mask could include other reactive metals such as copper, iron and nickel and their compounds.

10 The method also includes exposing a hard mask to a stream of oxidizing gas such as oxygen, nitrogen, fluorine, boron or carbon in the reactor prior to or during the etch step in order to form a compound with the reactive metal.

15 The method also includes exposing a hard mask to an ion or radical of oxygen, nitrogen, fluorine, boron or carbon in the reactor prior to or during the etch step in order to form an oxide, a nitride, a fluoride, a boride or a carbide or some combination of the preceding on the reactive metal.

20 The hard mask can also include any materials that are compatible with semiconductor fabrication processes, and semiconductor manufacturing tools and equipment which have the characteristics described herein.

25 The invention further includes selecting a hard mask which has or can develop an oxide, nitride, fluoride, carbide, or boride, or some combination of a reactive metal.

In another aspect of the invention, the method includes increasing the rate that one of an oxide, a nitride, a fluoride, a boride or a carbide forms on the hard mask in order to slow down the rate of erosion of the hard mask.

The invention further includes selecting a hard mask that is comprised of a metal which has a low sputter yield.

A further aspect of the present invention is to provide a method for containing critical dimension growth during an etching process including the step for placing a wafer or other substrate, for making by way of example only, a semiconductor product, a magnetic head or a flat panel display, with a hard mask disposed over a layer to be etched in a reactor, wherein the hard mask has at least one of a low sputter yield and a low reactivity to the etch chemistry of the etch process.

Accordingly, it is an object of the present invention to contain, control and minimize the growth of the critical dimension of a feature being etched.

It is still a further object of the present invention to perform the methodology of controlling and minimizing the critical dimension growth of a feature during an etch process, whether the process be conducted at low (below atmospheric) pressure, atmospheric pressure, or high (above atmospheric) pressure.

Other objects, advantages and features of the invention will be described herein and evidenced in the claims and figures.

#### **Brief Description of the Figures**

Fig. 1 depicts a schematical representation of a side elevational view of a wafer with a starting photoresist pattern placed over a hard mask, with the hard mask placed over the material to be etched.

Fig. 2 depicts a schematical representation similar to Fig. 1 which has been etched in order to define the hard mask layer.

Fig. 3 depicts a feature similar to Fig. 2 which has been etched to define the pattern in the material lying under the hard mask.

Fig. 4 depicts a schematical representation of an etch reactor wherein the method of the present invention can be carried out.

**Detailed Description of the Preferred Embodiment**

5           The method of the present invention can be performed in an etch reactor such as the etch reactor depicted in Fig. 4. It is to be understood that other reactors including but not limited to other etch reactors can be used and be within the spirit and scope of the invention.

10           The etch reactor of Fig. 4 is identified by the number 20 and is configured as a multi-frequency, tri-electrode reactor. The etching apparatus 20 includes a housing 22 and an etching chamber 24. A wafer 26 is positioned on a chuck incorporated into a bottom electrode 28. The chamber 24 further includes a side peripheral electrode 30 and an upper electrode 32. In a preferred embodiment, the side peripheral electrode 30 can be grounded or allowed to establish a floating potential as a result of the plasma developed in the chamber 24. The upper electrode 32 is generally grounded, but could also be designed to have a floating electrical potential. In typical operation, both the side peripheral electrode 30 and the upper electrode 32 are grounded as shown in Fig. 4.

15           Preferably two AC power supplies, first power supply 34 and a second power supply 36, are connected to the bottom electrode 28 through an appropriate circuitry 38, which can include by way of example only, matching networks and a combiner. Further a controller 20 40 controls the sequencing of the first and second AC power supplies 34, 36. Typically for this particular example only, the first power supply 34 operates in the kilohertz range and is optimally provided at about 450 KHz, and typically in the range of less than 500 KHz. The second power supply 36 operates in the megahertz range, and typically

operates at about 13.56 MHz, although other frequencies about above 1 MHz and also multiples of 13.56 MHz can be used with the present invention. The power supply 34 is powered at 200 watts and the second power supply 36 is powered at 500 watts for this example. Ion energy increases towards the kilohertz range while the ion density increases towards the megahertz range.

Additionally, reactor 20 includes gas inlet head 42 and a gas outlet port 44. Further, and preferably, the chuck 28 is heated so that a wafer positioned thereon is itself heated in the range of about 80°C to about 300°C during the process.

The growth in the critical dimension is attributable to the deposit of etched materials, mask materials, and/or compounds of etched materials, mask materials, and/or process gases on the sidewalls of the feature being etched and on the soft and/or hard masks. By way of example only, in a reactor for etching platinum with chlorine gas, materials which can stick to the sidewalls generally include platinum dichloride ( $\text{PtCl}_2$ ), a platinum trichloride ( $\text{PtCl}_3$ ), and/or other compounds. It is to be understood that the present process can be used more favorably for etching films comprised of platinum (Pt), copper (Cu), iridium (Ir), iridium dioxide ( $\text{IrO}_2$ ), lead zirconium titanate (PZT), ruthenium (Ru), ruthenium dioxide ( $\text{RuO}_2$ ), barium strontium titanate (BST), and bismuth strontium tantalate (Y-1 or SBT). These materials being etched are either metals or compounds which are of low volatility. Still other films and other semiconductor and non-semiconductor processes can benefit from this method.

Figs. 1-3 depict various stages of the inventive etch method using the reactor of Fig. 4. Fig. 1 represents a schematical representation of a scanning electron micrograph (SEM). In Fig. 1, the discrete upright structures represent the lithographic mask (a soft mask and in particular

a photoresist mask in this example) 50 which is patterned upon a hard mask 52 which has not yet been etched. The hard mask 52 has been deposited on layer 54, which is the material to be ultimately etched. Layer or film 54 is deposited on substrate 56.

In the embodiment of Fig. 1, the lithographic mask (soft mask) 50 is positioned on a hard mask 52, which hard mask is comprised of titanium nitride (TiN). The hard mask 52 is deposited on the layer 54 to be etched which in this embodiment is platinum (Pt). Layer 54 is deposited over a substrate 56 which can include, for example, silicon. The first step in the process is to etch the hard mask 52 into the desired pattern represented by the photoresist mask 50. The result of this process can be seen in Fig. 2. Fig. 3 depicts a representation where the platinum layer has been over-etched. Table 1 below records the changes in dimension in profile, pitch, feature, and space for the above four figures, where the pitch is equal to the feature dimension plus the space dimension. The change value is measured relative to the feature dimension of Fig. 1.

**Table 1**

**Pt Etch Process with Over-Etch**  
**0.025 $\mu$  CD gain with 79° profile (CD)**

	Profile	Pitch	Feature	Space	Change
Starting resist mask layer CD (Fig. 1)	79.2°	0.564 $\mu$	0.307 $\mu$	0.257 $\mu$	-
Starting TiN mask layer CD (Fig. 2)	66.7°	0.557 $\mu$	0.317 $\mu$	0.240 $\mu$	+0.010 $\mu$
Pt layer CD (Fig. 3)	78.9°	0.555 $\mu$	0.332 $\mu$	0.227 $\mu$	+0.025 $\mu$

The operating parameters for Table 1 using the reactor of Fig. 4 are as follows:

Pressure: 1 to 50 millitorr  
MHz Power: 110 to 1500 watts  
KHz Power: 0 to 500 watts  
Total Flow Rate: 10 to 500 SCCM  
HBR Flow Rate: 0 to 200 SCCM  
CL<sub>2</sub> Flow Rate: 0 to 200 SCCM  
O<sub>2</sub> Flow Rate: 0 to 200 SCCM

A similar platinum process yielded no CD gain and an 84° profile. The starting material for the hard mask was titanium. Dimensional features for this etching process are shown below in Table 2. The etching was allowed to proceed to over-etch. The operating parameters for this particular process are in accordance with those of Table 1. Table 2 demonstrates that the invention allows the critical dimension to be held steady, without any substantial growth during the etch process.

**Table 2**

**Pt Etch Process with Over-Etch  
0.00μ CD gain with 84° profile**

	Profile	Pitch	Feature	Space	Change
Starting resist mask layer CD	79.2°	0.564μ	0.307μ	0.257μ	-
Starting Ti mask layer CD	66.7°	0.557μ	0.317μ	0.240μ	+0.010 μ
Pt layer CD	84°	0.555μ	0.310μ	0.254μ	+0.003 μ

Generalizing from the above, the invention includes a method for containing critical dimension growth of a feature located on a wafer during an etch process wherein the wafer includes a hard mask comprised of a reactive metal or the oxide, nitride, fluoride, boride, or carbide, and/or combination thereof, of a reactive metal deposited over a layer to be etched. The oxide, nitride, fluoride, boride or carbide or combination thereof can be either (i) deposited as a layer, or (ii) formed in situ by exposing the reactive metal to a stream of oxygen, nitrogen, fluorine, boron or carbon and/or ions or radicals of the same either prior to or during the etch process. The hard mask layer thus acts as a self-passivation layer. In general, the class of reactive metals which are most appropriate of the present invention include titanium (Ti), aluminum (Al), and tantalum (Ta). Other reactive metals could include copper (Cu), tungsten (W), iron (Fe), nickel (Ni), cobalt (Co), and molybdenum (Mo). The most appropriate oxides and nitrides are titanium oxide ( $\text{TiO}_2$ ), aluminum oxide ( $\text{Al}_2\text{O}_3$ ), titanium nitride (TiN), tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ), and tantalum nitride (TaN). Metal analogs of fluorides, borides, and carbides are also appropriate.

Other metals which are reactive and readily form oxides, nitrides, fluorides, borides or carbides come within the spirit and scope of the invention. Further, these metals preferably have a low sputtering yield with etchants which further enhances critical dimension growth containment. Table 3 below compares the sputtering yield of these materials against platinum and silicon dioxide for argon ion bombardment at 600 electron volts (eV).

**Table 3**

	Bombarding argon ion energy in 600 eV
Pt	1.56
SiO <sub>2</sub>	1.34
Ti	0.58
TiO <sub>2</sub>	0.96
Al	1.24
Al <sub>2</sub> O <sub>3</sub>	0.18
Ta	0.62
Ta <sub>2</sub> O <sub>5</sub>	0.15
TiN	1.60
W	0.62

Adding oxidants such as oxygen to the process gas and in particular with respect to a hard mask comprised of titanium or aluminum causes the formation of an oxide on the hard mask resulting in less erosion of the hard mask and a minimization of the critical dimension growth. This oxidation of the metal results in less sputtering, which means that the hard mask itself can be thinner. Similar advantages occur with the formation of nitrides, carbides, and/or borides, and/or some combinations thereof of reactive metals.

Accordingly, it can be seen that reactive metals which form skins of oxides, nitrides, fluorides, borides and/or carbides are advantageous to the method of the invention. Further, increasing the temperature at the surface of the wafer, in preferably the range of 80° Centigrade to 300° Centigrade, increases the rate of oxidation which slows the erosion rate of the hard mask. Again, similar results are observed with oxides, nitrides, fluorides, carbides, and/or borides, and/or combinations thereof, of reactive metals.

Thus, from the above, it can be seen that the hard mask selected from a reactive metal or selected from an appropriate oxide, nitride, fluoride, carbide, boride, or some combination thereof, of a reactive metal, and which material has a favorably low sputter yield, is an appropriate material for the hard mask of the present invention. Such method is particularly important for controlling critical dimension growth for a submicron feature and in particular for features which have a pitch of less than  $0.5\mu$ .

Further, it is to be understood that for the above preferred hard mask, a low sputter yield, and a low chemical reactivity of the mask with the process gases is a consideration. For example, from Table 3, a quick review would tend to suggest that titanium with a sputter yield of 0.58 would be a more appropriate hard mask than titanium oxide with a sputter yield of 0.96. However, with etchant gas of chlorine, the titanium is more reactive than the titanium oxide and thus, the titanium oxide could provide for better critical dimension growth containment even though it has a higher sputter yield.

#### **Industrial Applicability**

From the above, it can be seen that the method of the invention is useful for performing an etch or other semiconductor process step while containing critical dimension growth in order to develop features for submicron dimension products.

Other features, aspects and objects of the invention can be obtained from a review of the figures and the claims.

It is to be understood that other embodiments of the invention can be developed and fall within the spirit and scope of the invention as claimed.